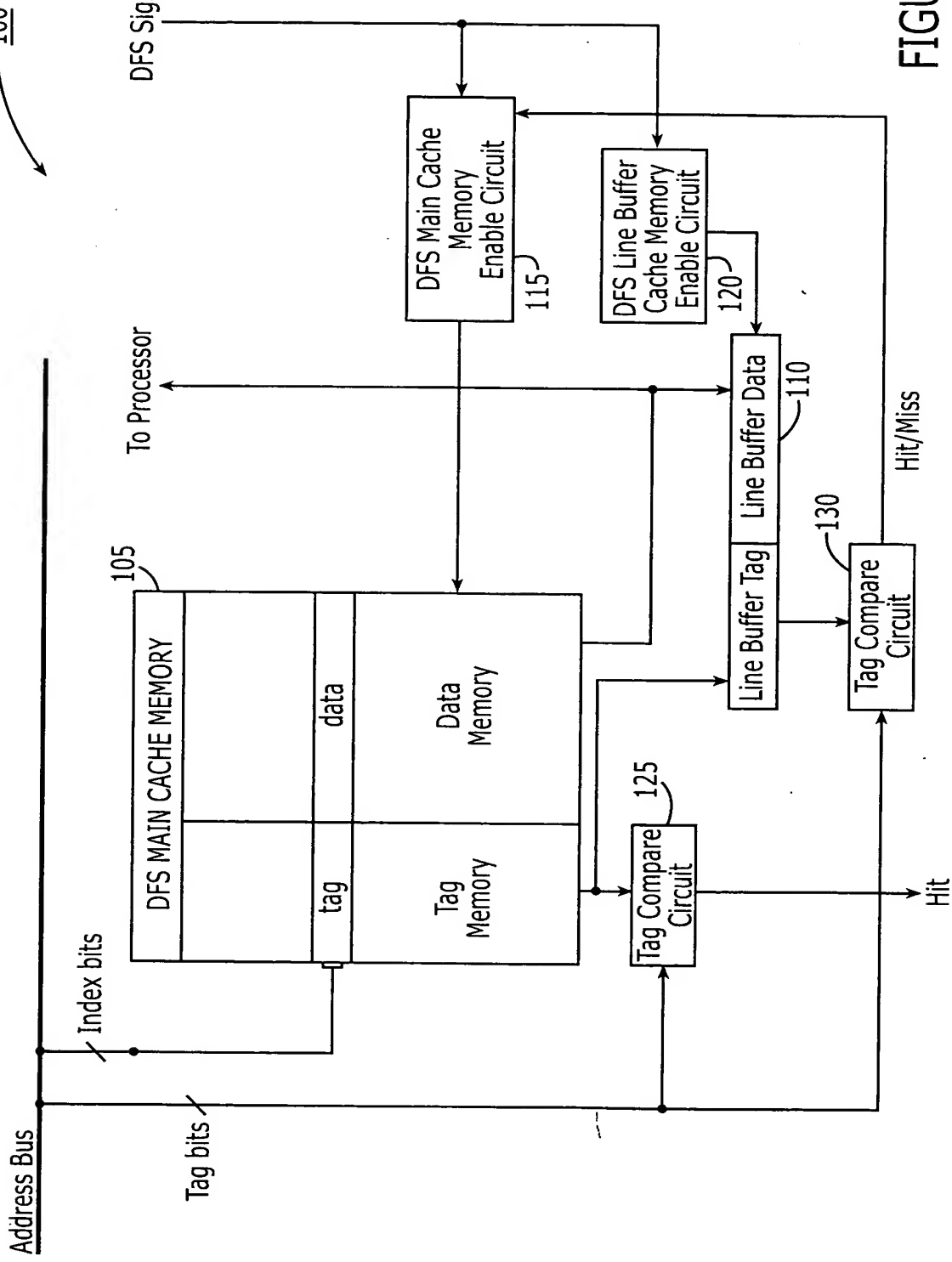
100
DFS Signal
DFS Main Cache Memory Enable Circuit
115
DFS Line Buffer Cache Memory Enable Circuit
120
To Processor
Line Buffer Data
110
Hit/Miss
105
DFS MAIN CACHE MEMORY
data
Data Memory
tag
Tag Memory
Line Buffer Tag
130
Tag Compare Circuit
125
Tag Compare Circuit
Hit
Index bits
Address Bus
Tag bits

FIGURE 1

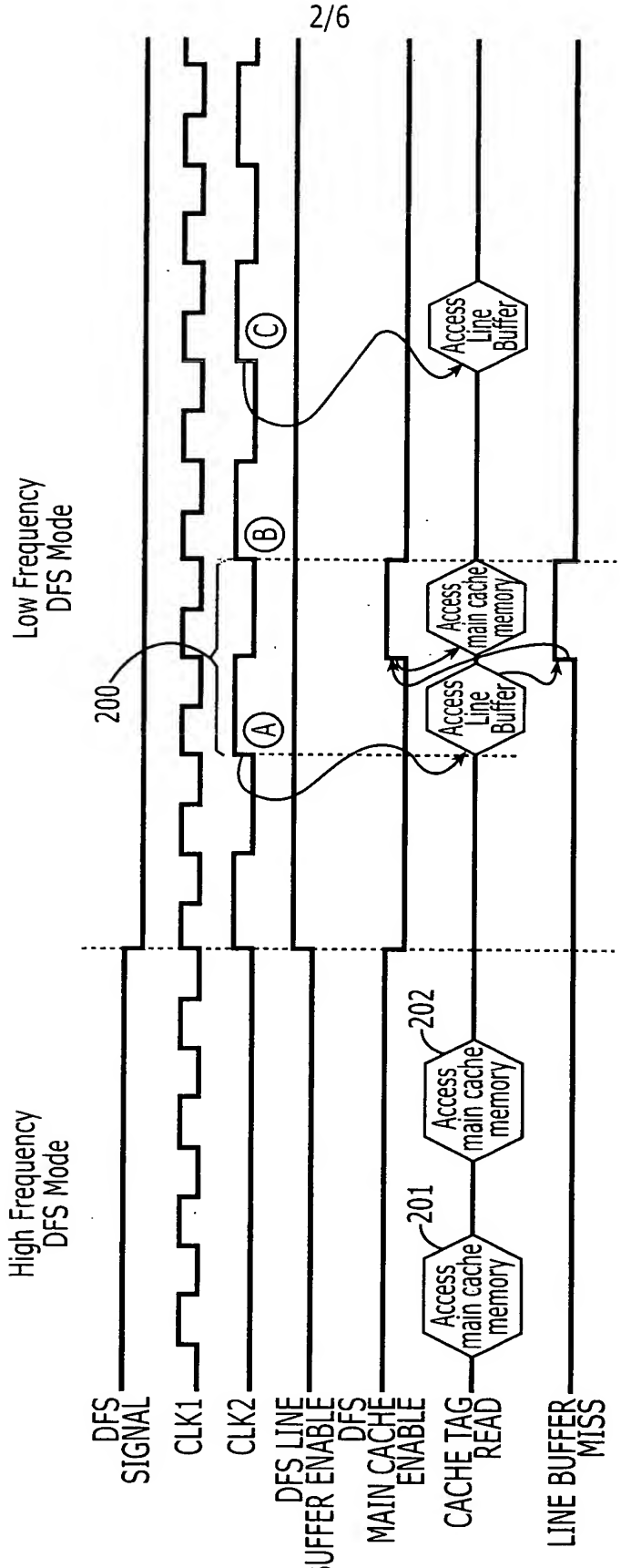
High Frequency DFS Mode
Low Frequency DFS Mode
200
201
202
A
B
C
DFS SIGNAL
CLK1
CLK2
DFS LINE BUFFER ENABLE
DFS MAIN CACHE ENABLE
CACHE TAG READ
LINE BUFFER MISS
Access main cache memory
Access Line Buffer
Access main cache memory
Access Line Buffer
Access main cache memory

FIGURE 2

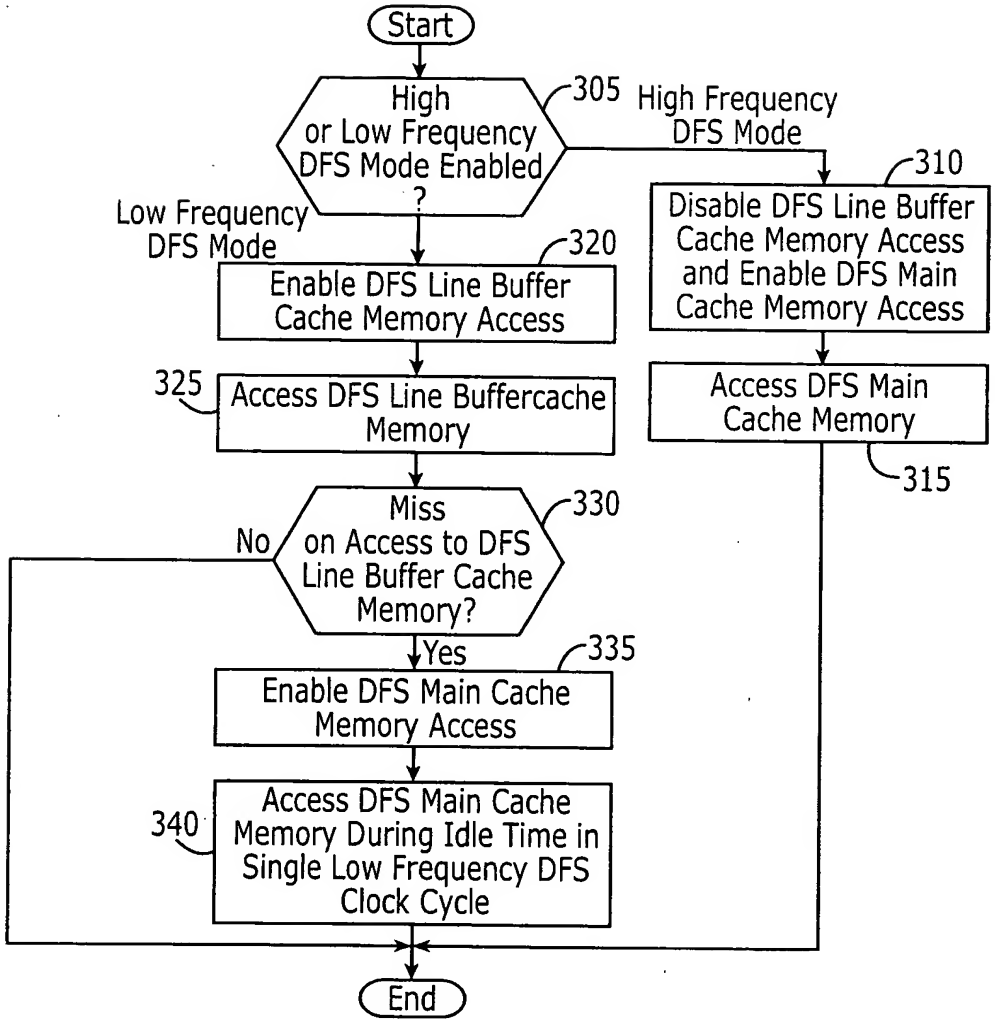
Start
High or Low Frequency DFS Mode Enabled ?
305
High Frequency DFS Mode
310
Disable DFS Line Buffer Cache Memory Access and Enable DFS Main Cache Memory Access
Low Frequency DFS Mode
320
Enable DFS Line Buffer Cache Memory Access
325
Access DFS Line Buffercache Memory
Access DFS Main Cache Memory
315
Miss on Access to DFS Line Buffer Cache Memory?
330
No
Yes
335
Enable DFS Main Cache Memory Access
340
Access DFS Main Cache Memory During Idle Time in Single Low Frequency DFS Clock Cycle
End

FIGURE 3

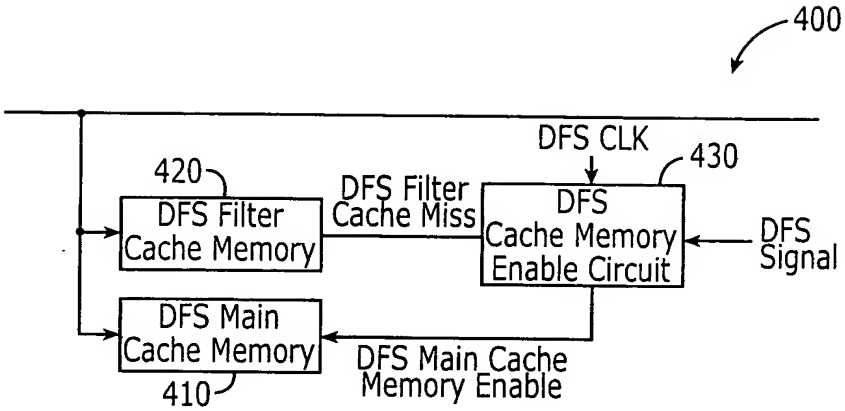

FIGURE 4

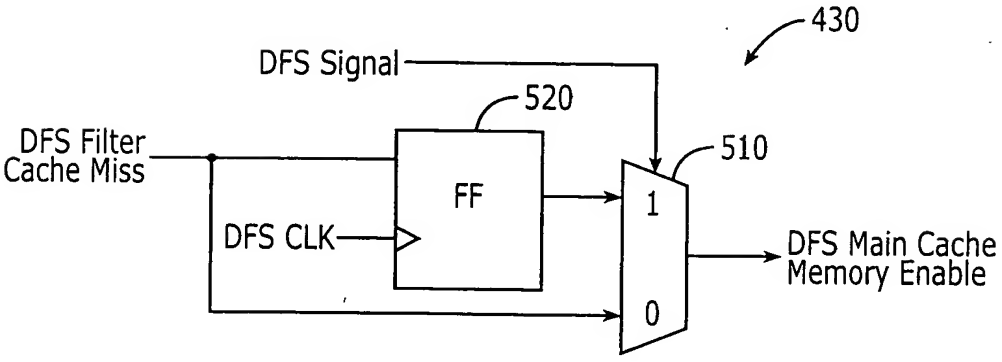

FIGURE 5

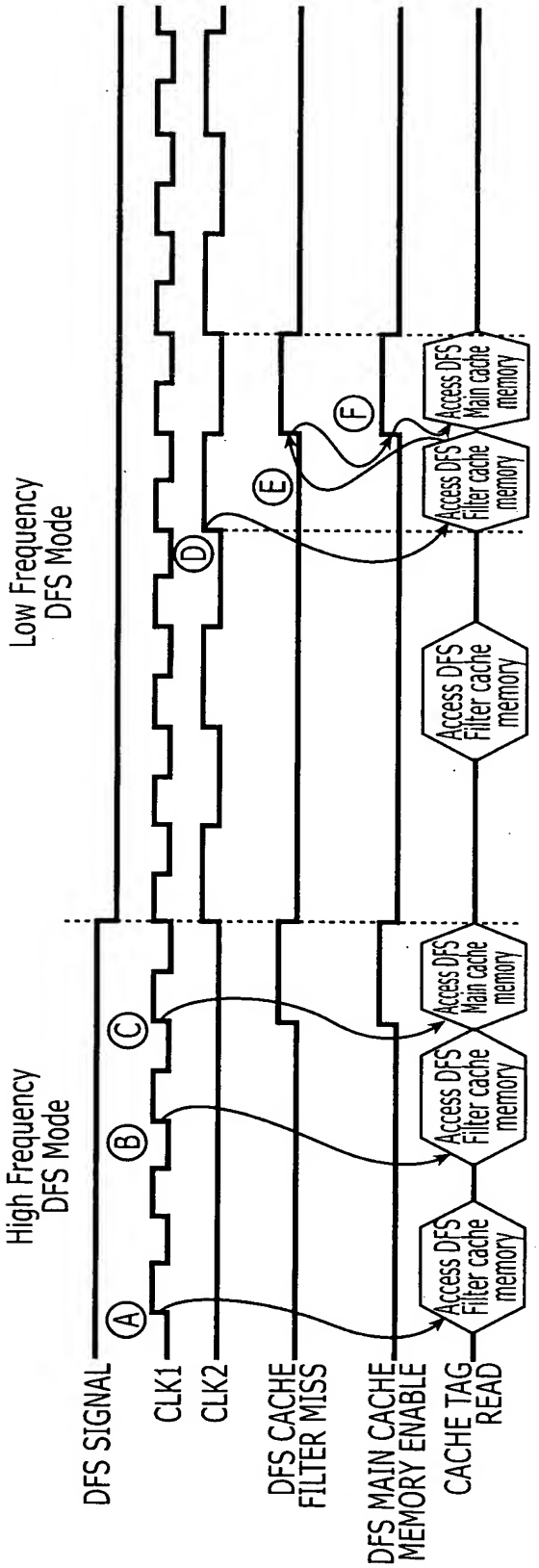
High Frequency DFS Mode
Low Frequency DFS Mode
DFS SIGNAL
CLK1
CLK2
DFS CACHE FILTER MISS
DFS MAIN CACHE MEMORY ENABLE
CACHE TAG READ
A
B
C
D
E
F
Access DFS Filter cache memory
Access DFS Main cache memory
Access DFS Filter cache memory
Access DFS Main cache memory
Access DFS Filter cache memory
Access DFS Main cache memory

FIGURE 6

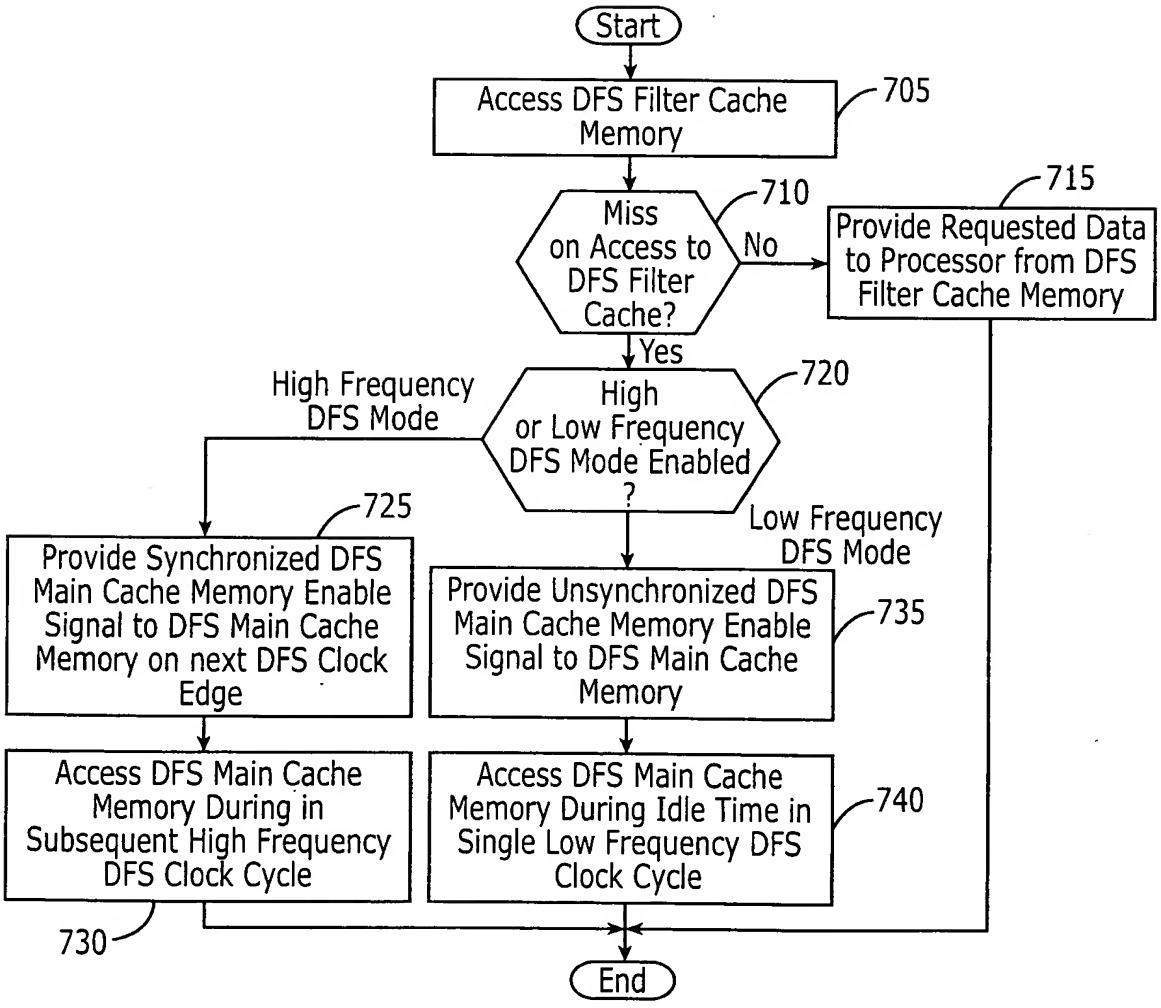
Start
Access DFS Filter Cache Memory
705
Miss on Access to DFS Filter Cache?
710
No
Provide Requested Data to Processor from DFS Filter Cache Memory
715
Yes
High or Low Frequency DFS Mode Enabled ?
720
High Frequency DFS Mode
Low Frequency DFS Mode
Provide Synchronized DFS Main Cache Memory Enable Signal to DFS Main Cache Memory on next DFS Clock Edge
725
Provide Unsynchronized DFS Main Cache Memory Enable Signal to DFS Main Cache Memory
735
Access DFS Main Cache Memory During in Subsequent High Frequency DFS Clock Cycle
Access DFS Main Cache Memory During Idle Time in Single Low Frequency DFS Clock Cycle
740
730
End

FIGURE 7